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DIGITAL SIGNAL PROCESSING

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DIGITAL SIGNAL PROCESSING

Semiannual Technical Report
covering the period
July 15, 1973 - January 15, 1974

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Semiannual Technical Report

ONR Contract N00014-67-A-0204-0064

covering the period July 15, 1973 - January 15, 1974

submitted by

A. V. Oppenheim - Principal Investigator

February 26, 1974

Projects Studied Under the Contract:

During the second half of the contract year, the program continued the following studies: development of a high speed digital processor for speech synthesis, design of two-dimensional recursive digital filters, reconstruction of multi-dimensional signals from their projections, signal analysis by cepstral prediction, speed transformations of speech, and the hardware implementation of a non-recursive digital filter. These projects are summarized in the following pages and a list of available publications is appended.

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Abstract

During the second half of the contract year, the program continued the following studies: development of a high speed digital processor for speech synthesis, design of two-dimensional recursive digital filters, reconstruction of multi-dimensional signals from their projections, signal analysis by cepstral prediction, speed transformations of speech, and the hardware implementation of a non-recursive digital filter. These projects are summarized in the following pages and a list of available publications is appended.

REPORT SUMMARY

I. Digital Signal Processing Computer (The Black Box)

The detailed design (at the chip level) of the Black Box is now complete except for the Direct Memory Access Logic which is being purposely delayed until careful timing measurements can be made. All ECL chips, except for a small number of MC10181 ALUs, have been received, and checkout of the Fairchild 95415 1K RAM memory chips is in progress. The 24 x 24 bit multiplier has been completely simulated and optimized on a PDP-9 computer. The final speed is 120 nsec which is slightly higher than expected, but the ALU chip was held to 155. All circuit boards have been received from Augat, but short pins on some of them have necessitated local modifications.

We are now at the layout and wiring stage. The entire machine will first be laid out manually. Considerable effort is now being expended to learn to use the Stanford design aid system which is currently running on the MIT AI group PDP-10. This system will provide documentation via the XGP printer, and a card deck for automatic wiring. While we are somewhat behind on our wiring schedule, we feel that the use of appropriate design aids will pay off by providing editing facilities and high-quality documentation.

II. Two-Dimensional Recursive Digital Filter Design

Current work on the design of two-dimensional recursive digital filters is virtually complete and will be published as an M.I.T. doctoral dissertation [Dan Dudgeon: Two-Dimensional Recursive Filtering] to be submitted in May 1974. Furthermore, various subtopics will be published in RLE Quarterly Progress Reports later this spring.

The final results of this study are essentially the same as those described in our last report [July 1973]. The greatest number of frequency constraint points which has been used in design examples remains at 544 due to limitations of computer memory and the availability of processing time. And, there still remains to be solved the fundamental mathematical problem of factoring (analytically) the designed magnitude-squared function which has been treated, to date, only in an approximate sense.

Moreover, the research effort on one-dimensional recursive filter design mentioned in the previous report is also complete. The results appear to be quite good and have been applied successfully to the design of filters with arbitrary frequency responses and arbitrary error weightings. A paper based on this work has been submitted for publication to the IEEE Trans. on Acoustics, Speech, and Signal Processing [Dan Dudgeon: "Recursive Filter Design Using Differential Correction."]

III. Reconstruction of Multi-Dimensional Signals from their Projections

An invited paper [Mersereau and Oppenheim] on the reconstruction of multi-dimensional signals from their projections has been prepared and submitted to the Proceedings of the IEEE. This paper is a tutorial review of the reconstruction problem and some of the algorithms which have been proposed for its solution. In addition, a number of new algorithms which have been developed in the course of this research are given and some of the advantages of these algorithms over previous algorithms are discussed. Some comparisons of these algorithms applied to reconstructions of two-dimensional pictures are given. Furthermore, a number of new theoretical results are presented relating to the minimum number of projections necessary for exact reconstruction.

Further work in the area of multi-dimensional processing is continuing under this contract. Some preliminary results have been reported [Mersereau] at the Arden House Workshop on Digital Signal Processing.

IV. Cepstral Prediction

A new technique called cepstral prediction has been developed which is useful for analyzing the class of signals whose z-transforms can be modeled as rational functions of z. Using this approach, both the poles and zeros of the signal model can be estimated. Initial results of this work have been published [Oppenheim and Tribolet] and have also been presented at the Arden House Workshop on Digital Signal Processing.

Briefly, the technique of cepstral prediction is the following. Given a signal whose z-transform can be modeled as rational in z, its complex cepstrum is computed. Using the familiar techniques of linear prediction, the poles of the cepstrum can be estimated. Since the cepstrum has the property that the locations of its poles correspond to the locations of the poles and zeros of the original signal, the problem of determining the locations of the poles and zeros of a given signal reduces to the problem of deciding which of the poles of the cepstrum correspond to poles of the original signal and which correspond to zeros. Several such decision algorithms are presently under investigation.

V. Speed Transformations of Speech

Recently, a new research program has been undertaken in the area of speed transformations of speech. That is, the modification of a speech signal in such a manner that its speed is changed while its intelligibility and natural quality is preserved.

The first step in the development of such a system is the implementation of a high quality analysis/synthesis scheme for speech. The design criteria for such a system differ from the traditional points of view in vocoder design in that efficient coding and bit-rate reduction are not important considerations. Rather, what is required is an extremely high quality parametric representation of the speech waveform. Moreover, it would be advantageous if the parameters chosen to represent the speech signal could be related to the physical mechanism of speech production; for such a representation naturally lends itself to the imposition of articulatory rules. For this reason, current attention is focused on the development of an analysis/synthesis scheme based on linear prediction because from the predictor coefficients it is possible to derive an acoustic-tube analog for resynthesis of the speech signal. The model implied by linear prediction, however, has certain shortcomings (for example, it assumes an all-pole model for the speech production system) and it is therefore the immediate objective of this research to study the results of applying the linear-prediction model to high quality speech and to develop suitable improvements so as to more accurately represent the speech waveform.

VI. Hardware Implementation of a Non-Recursive Digital Filter

The direction of this research is to investigate the considerations in the implementation of non-recursive digital filters, and to carry out the implementation of a flexible non-recursive digital filter which can be used to study further the hardware considerations for this class of filters. The considerations in the implementation of our filter have been divided into four areas: multipliers, architecture, storage and interfaces.

The multiplying scheme used in a non-recursive digital filter is a major factor in establishing the filter's bandwidth, order, and cost relationships. The bandwidth of our filter was set at twenty kilohertz (2×10^4 Hz) in order to process high fidelity audio signals. The data sampling period was, therefore, twenty five microseconds (25×10^{-6} sec). The order-cost relationship was then established. Using this information, we decided on and are presently building a sixteen by twelve bit array multiplier with a multiplying time of four hundred nano-seconds (400×10^{-9} sec). Under this speed and bandwidth constraint, the maximum order of the filter is sixty three (63).

The architecture of the filter is not yet fully established; but at present, two functions have been determined. The filter will be able to be operated as a one hundred and twenty seventh (127) order linear phase filter, and the filter will have variable coefficient (up to 16 bits) and data (up to 12 bits) wordlengths.

The storage element for data and coefficients will be random access memory rather than the seemingly more natural choice of shift register memory. Random access memory is the logical choice for coefficient storage since it does not suffer from the potential loss of information as does continuously recirculated shift register memory. Random access memory also requires considerably less control hardware when operating as data storage for a linear phase filter.

The interfaces for data will be 12 bit A/D input, and 12 bit D/A output. In order to realize a linear phase filter with minimum hardware control, the digital representation for data will be in fractional twos-complement form. To allow for the maximum flexibility in the inputting of coefficients, it is our present intention to be able to interface our filter to both a general purpose computer through a teletype port for on-line use, and our Hewlett Packard Model 9830 calculator indirectly through a compatible cassette tape system. Coefficients will also be inputted through the front panel using a fractional sign-magnitude decimal format, thus facilitating human interaction. The digital representation for coefficients will be in fractional sign-magnitude form, thereby minimizing interface hardware.

In summary, the proposed filter will be a sixty-third order (one hundred twenty seventh order when used as a linear phase filter) non-recursive digital filter having variable coefficient and data wordlengths. It will be implemented using an array multiplier and random access memory. On-line interfacing with a

computer will be provided through a standard teletype port, while long storage of coefficients will be provided by a cassette tape system compatible with a HP Model 9830 calculator. Front panel controls will allow for the inputting of coefficients in convenient decimal form.

Publications Supported Under ONR Contract N00014-67-A-0204-0064 through January, 1974

1972 R. Mersereau, "Recent Advances in the Theory of Reconstructing Multi-Dimensional Signals from Projection," Quarterly Progress Report 105, M.I.T., Research Laboratory of Electronics, April 1972, pp. 169-183.

A. V. Oppenheim, D. Johnson, "Discrete Representation of Signals," Proc. IEEE, Vol. 60, No. 6, June 1972, pp. 681-691.

M. R. Portnoff, V. W. Zue, and A. V. Oppenheim, "Some Considerations in the Use of Linear Prediction for Speech Analysis," Quarterly Progress Report No. 106, M.I.T., Research Laboratory of Electronics, July 15, 1972, pp. 141-150.

A. V. Oppenheim and C. J. Weinstein, "Effects of Finite Register Length in Digital Filtering and The Fast Fourier Transform," Proc. IEEE, Vol. 60, No. 8, pp. 957-976, August 1972.

C. Braccini and A. V. Oppenheim, "Applications of Digital Frequency Warping to Unequal Bandwidth and Vernier Spectrum Analysis," Proceedings Florence Seminar on Digital Filtering, September 21, 22, 1972, pp. 137-141 (also, Conference on Signal Processing, University of Erlangen, Erlangen, Germany, April 4-6, 1973).

R. M. Mersereau, "The Digital Reconstruction of Multi-Dimensional Signals from Their Projections," Proc. 10th Annual Conference on Circuit and System Theory, Monticello, IL, October 4-6, 1972, pp. 326-334.

1973 A. V. Oppenheim, "Some Digital Signal Processing Activities at M.I.T.," Conference on Signal Processing, University of Erlangen, Erlangen, Germany, April 4-6, 1973.

A. V. Oppenheim, "Homomorphic Deconvolution," Proc. "Seminaire G.U.T.S." Centre d'Etudes Nucléaires de Grenoble, Grenoble, France, June 14-15, 1973.

A. V. Oppenheim and J. Tribolet, "Pole-Zero Modelling Using Cepstral Prediction," Quarterly Progress Report No. 111, M.I.T. Research Laboratory of Electronics, Oct. 15, 1973, pp. 157-159.

R. Mersereau, "Recovering Multi-Dimensional Signals from Their Projections," Computer Graphics and Image Processing, (in press).

R. M. Mersereau, "An Algorithm for Performing an Inverse Chirp Z-Transform," IEEE Trans. on Acoustics, Speech, and Signal Processing, (in press).

Papers Submitted for Publication

D. E. Dudgeon, "Recursive Filter Design Using Differential Correction," (IEEE Trans. on Acoustics, Speech, and Signal Processing).

R. M. Mersereau and D. E. Dudgeon, "The Representation of Two-Dimensional Sequences as One-Dimensional Sequences," (IEEE Trans. on Acoustics, Speech and Signal Processing).

R. M. Mersereau and A. V. Oppenheim," Digital Reconstruction of Multi-Dimensional Signals from their Projections," (Proceedings of the IEEE)(invited paper).

C. Braccini and A. V. Oppenheim, "Unequal Bandwidth Spectral Analysis Using Digital Frequency Warping," (IEEE Trans. on Acoustics, Speech, and Signal Processing).